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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, April 2015
(2013 Scheme)
13.305 : DIGITAL SYSTEM DESIGN (FR)

Time: 3 Hours Max. Marks: 100

PART – A

Answer **all** questions. **Each** question carries **2** marks.

1. Simplify the following expression :

   a) $y = (A + B)(A + C')(B' + C')$

   b) $T = AB + (AC)' + AB'C(AB + C)$.

2. Design basic gates (AND, OR, NOT) using 2 x 1 multiplexer.

3. How will you implement a full subtracter using full adder and gates ?

4. List the difference between Synchronous reset and Asynchronous reset.

5. Give the circuit to extend falling edge of the input by 2 clock pulse.

6. Differentiate between Mealy and Moere machine.

7. Draw the logic diagram of SR latch using NOR gates. Also give its excitation table.

8. List major differences between PLA and PAL.

9. How divide overflow problem can be avoided ?

10. Why should sign of the remainder after a division be the same as the sign of the dividend.

(10×2=20 Marks)

P.T.O.

PART – B

Answer **one full** question from **each** Module. **Each** question carries **20** marks.

Module – I

11. a) Design a 8-bit odd parity detector. 4

    b) Design a combinational circuit with three inputs x, y and z and three outputs A, B, C. When the i/p binary is 0, 1, 2 or 3 the binary o/p is one greater than i/p. When the binary i/p is 4, 5, 6 or 7 the binary o/p is one less than i/p. 10

    c) Realize the circuit using NAND gates alone.
    $f = A'B + B'C + A'C'$. 6

OR

12. a) Design a combinational circuit that will convert BCD codes into corresponding Excess three codes. 10

    b) Minimize the function $A = \Sigma(2, 3, 7, 10, 12, 22, 27, 30, 31) + \phi(8, 11, 14, 28, 29)$ where ϕ denotes don't care condition, using Quine McCluskey method. Realize the circuit using NOR gates. 10

Module – II

13. a) Implement the functions using : 10
    i) 4×1 MUX
    ii) 3×8 decoder.
    A) F(X Y Z) = {0, 2, 4, 7}
    B) T(A B C) = {1, 2, 6}.

    b) Design a 4 bit carry look ahead adder. 10

OR

14. a) Design a 3 bit universal shift register. 10

    b) Construct a state diagram for a more sequential circuit that will detect the serial input sequence X = 010110. When the complete sequence has been detected, then cause output 2 to go high. The input sequence may overlap and circuit should be able to detect overlaps. Also design the circuit using D flip flops. 10

Module – III

15. a) Design a counter that counts in sequens 0, 1, 5, 3, 7 and repeat the sequence. Use T flip flops. 10

    b) Design a circuit using ROM that generates Fibonacci series upto 10 bit. 10

OR

16. a) Design a BCD subtracter using PLA. 10

    b) Design an up/down 3 bit synchronous counter using D flipflops. 10

Module – IV

17. a) Derive an algorithm in flow chart form for adding and substracting two fixed point binary numbers when negative numbers are in signed 1's compliment representation. 10

    b) Show that there can be no mantissa over flow after a multiplication operation. 10

OR

18. a) Formulate a hardware procedure for detecting an overflow by comparing the sign of augend and addend. The numbers are in signed twos compliment representation. 10

    b) Derive an algorithm in flow chart form for the restoring method of fixed point division. 10